

12. Sync generator - unit 2

12.1 General

Unit 2 generates a number of signals without which the instrument cannot function. These can either be locked to an external video signal or to the TCXO reference oscillator on unit 1. In addition, information (pin connections, description, etc.) is provided about the two integrated circuits, the SAA1043 and SAA1044, which play an important part in the operation of this unit.

12.2 Description

The sync generator is built up around the SAA1043 (V19). This IC has a built-in 5MHz oscillator (5.03MHz M-PAL and NTSC-versions) from which a number of sync signals are derived. This oscillator is locked to either the line sync pulses of an external video signal, or to the internal TCXO reference oscillator via SAA1044 genlock IC in order to obtain correct subc/line relationship.

If an external sync signal is present it is fed via the chroma take out circuit and the clamp circuit to the sync peak detector. This circuit detects if the incoming sync is missing or decides whether its level is too low. If the level is below 6dB from nominal value, the detector gives information to the sync IC (SAA1043) via the Int/Ext signal selector circuit. The sync generator shifts to internal mode, and locks to the TCXO on unit 1.

SAA1044 (V27) is the heart of the subcarrier genlock circuit. It is provided with two built-in oscillators at f_{SUBC} . The oscillator A is locked to the TCXO reference oscillator on unit 1 in internal mode. In external mode it is locked to either the burst of an external video signal, or to the line sync. The subcarrier may also free run, internally selectable by jumper. The oscillator B is locked to oscillator A.

If an external video signal is present, the burst of this signal is fed to the burst level detector. This circuit detects if the burst is missing or decides whether its level is too low. If the level is below 6dB of no-

minimal value the subcarrier reference select circuit is either free-running or locked to the line sync.

If the subcarrier is genlocked to an external source, the TCXO on unit 1 is switched off to prevent noise due to interaction of the two frequencies. This function is controlled via the SUGE signal.

Proper subc/line relationship is maintained by using the two signals FH3 and FH80 from the SAA1043. These are fed to the line/subc phase detector circuit in the SAA1044 where they are compared with the internal subcarrier signal from oscillator A. The output of this circuit (PH.A) is fed to the sync lock filter where it controls the 5MHz (or 5.03MHz) oscillator in the sync IC.

If an external sync signal is applied, the subc/line relationship is referenced to the external signal if a burst is present.

The small crash-lock unit underneath the sync IC (V19) consists of two flip-flops. The first flip-flop detects if there is an external sync present. If no sync is applied the second flip-flop stops the internal line counter in the sync generator IC (V19) until an external vertical sync pulse is applied on the V1 line.

12.3 SAA1043 sync generator chip description

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment. The device is programmable to suit different TV standards with the aid of three program inputs (FD, X, Y).

12.3.1 Functional description

The SAA1043 is provided with a built-in oscillator. The oscillator can work with an external LC-circuit or a crystal.

The following frequencies are applied to the clock input (OSCI):

G,N-PAL : 5.0MHz

M-PAL/NTSC : 5.034964MHz

An other circuit makes it possible to lock the internally generated sync signal to an external sync signal.

This functions as follows:

Reset pulses are derived from each falling edge of the external sync signal (ECS). This resets the sync counter which is clocked by a pulse from the horizontal counter. The ECS is compared with the internally generated horizontal sync pulse in the phase comparator.

If a phase difference between the two signals is detected, the output (PH) is pulled towards the Vdd or Vss dependent on the direction of the error. The phase error voltage (PH) is used to correct the frequency of OSCI via VCO and nullifies the phase error between internal and external signals. Equalization and serration pulses do not effect the phase comparator.

A no sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no sync signal (NS) occurs 6.4 μ s after the time of the missing reset pulse.

Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulation the DL ($2xf_H$) input to the vertical counter via the addition/subtraction logic. Note that the crash-lock circuit override this function.

12.4 SAA1044 subcarrier coupler description

The subcarrier coupling IC SAA1044 is designed in combination with the universal sync IC SAA1043 for applications involving cameras, film scanners, signal generators, and associated equipment. The use of this IC is necessary when an exact relationship between the subcarrier and line frequency is desired.

The TV standard required for operation is programmed by use the inputs FX, X, and FH3 as shown in the following schedule.

Standard	FD	X	FH3	Relationship of subcarrier frequency (f_s) to horizontal scan frequency (f_H)
G-PAL	0	1	400Hz	$f_s = 283.7516f_H$
N-PAL	1	1	400Hz	$f_s = 229.2516f_H$
M-PAL	1	0	1	$f_s = 227.25f_H$
M-NTSC	1	0	0	$f_s = 227.5f_H$

Positive logic: 1 = HIGH; 0 = LOW

$80f_H$ is used as a reference frequency for the line frequency f_H ; this frequency is delivered by the sync IC for all standards.

The f_{SUBC} is derived from an on-chip oscillator, which can work with a crystal or with LC elements. Both frequencies are compared by phase comparator 1. The output signal of this phase comparator can be fed to a low-pass filter, which supplies the control voltage for a VCO.

Either the subcarrier or line oscillator frequency can be chosen as a reference. The filter can be active or passive depending on the application.

For genlock applications a third phase detector is provided with high accuracy and stability. This phase detector is used for comparing the internal subcarrier and external reference frequency.

To adjust the phase, a phase detector with a linear characteristics is provided.

Control of the phase is achieved by comparing the average value with a reference voltage.

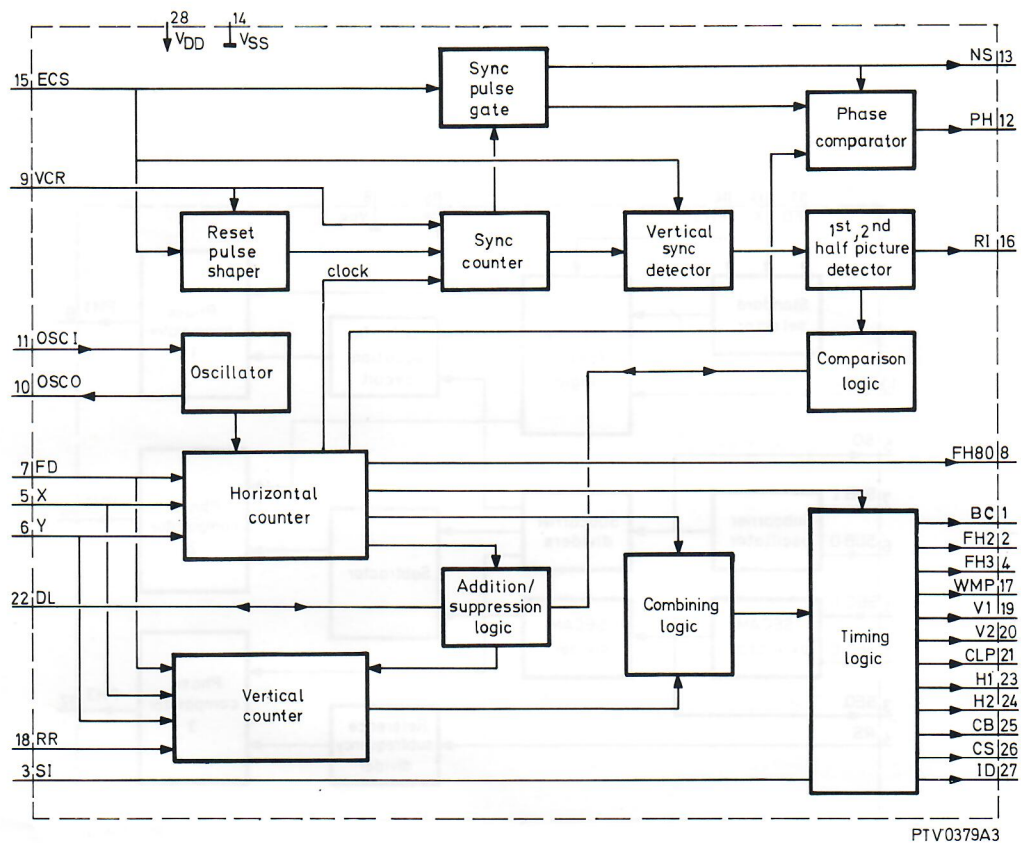


Fig. 12-1 SAA1043 internal block diagram

BURST FLAG/CHROMA BLANKING (SECAM)

PAL IDENTIFICATION

SET IDENTIFICATION (PAL, PAL-M, SEC)

400Hz-PAL, 360Hz-NTSC PAL-M, FH/3 (SECAM)

STANDARD SWITCH

STANDARD SWITCH

STANDARD SWITCH (FIELD DIVIDER)

 $80 \times f_H$

VCR/STANDARD

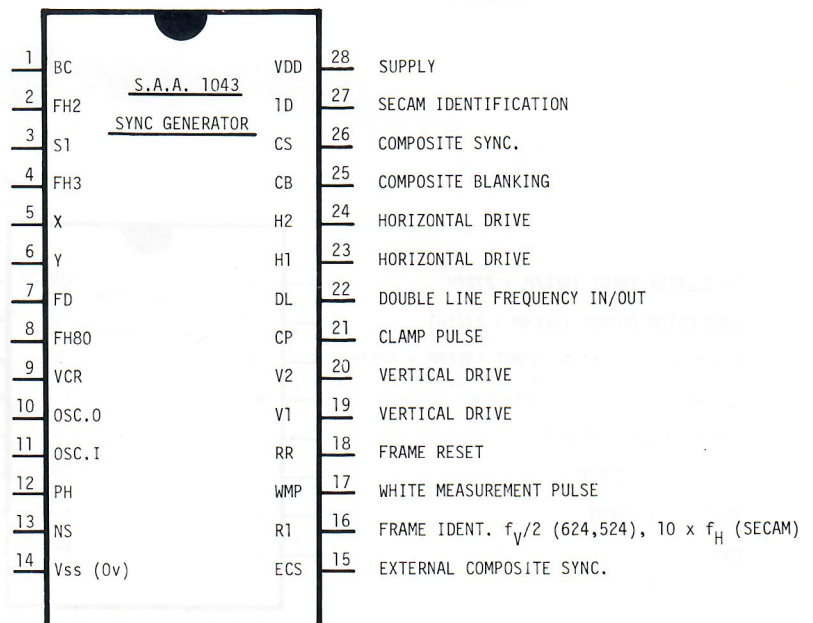
OSCILLATOR OUTPUT

OSCILLATOR INPUT

PHASE DETECTOR

NO SYNC. DETECTOR

LOGIC GROUND



PTV0040A3

Fig. 12-2 SAA1043 pin connections/signal names

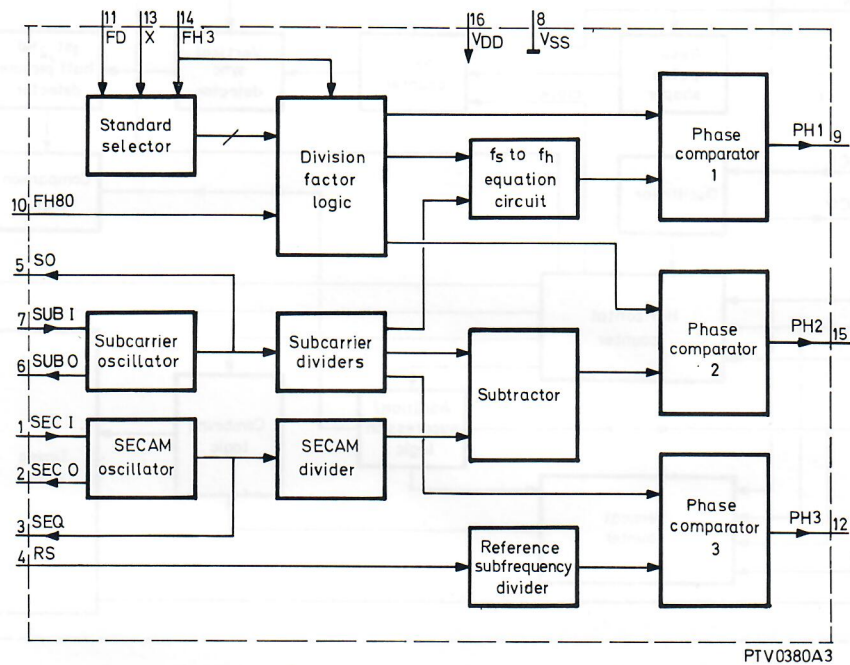


Fig. 12-3 SAA1044 internal block diagram

OSCILLATOR INPUT (SECAM = 272fH)

OSCILLATOR OUTPUT (SECAM = 272fH)

INVERTED OSCILLATOR OUTPUT (SECAM = 272fH)

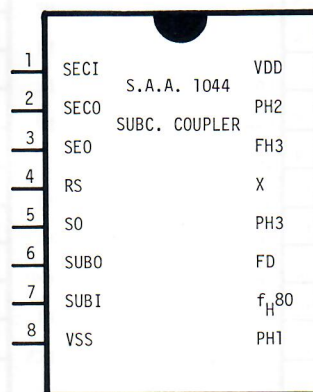
REFERENCE SUBCARRIER FREQUENCY

INVERTED OSCILLATOR OUTPUT

OSCILLATOR OUTPUT

OSCILLATOR INPUT

GROUND



SUPPLY

PHASE COMPARATOR OUTPUT (SEC I and fH80)

STANDARD SWITCH (400hz input from SAA1043)

STANDARD SWITCH

PHASE COMPARATOR OUTPUT (RS and SUB I)

STANDARD SWITCH (FIELD DIVIDER)

80 x fH INPUT (from SAA 1043)

PHASE COMPARATOR OUTPUT (fH80 and SUB I)

PTV0045A3

Fig. 12-4 SAA1044 pin connections/signals names

12.5 Test and adjustment

Measuring equipment :

Oscilloscope	: e.g. Philips PM 3055
Digital voltmeter	: e.g. Philips PM 2528
Test signal generator	: e.g. Philips PM 5640
Sc-H meter	: e.g. Philips PM 5668

Check that all configuration switches are correctly placed for the version in use.

(This information is found in Chapter 6 - Configuration).

12.5.1 Voltage checks

1. Using a digital voltmeter, check for $+8V \pm 0.4V$ on $\textcircled{1}$ (V6, pin8).
2. Using a digital voltmeter, check for $-8V \pm 0.4V$ on $\textcircled{2}$ (V6, pin4).
3. Using a digital voltmeter, check for $-5V \pm 0.2V$ on $\textcircled{3}$ (V25, pin16).
4. Using a digital voltmeter, check for $+5V \pm 0.2V$ on $\textcircled{4}$ (connector pin20 a,c).

12.5.2 Adjustments

1. Subcarrier output amplitude.

- Connect an oscilloscope terminated with 75Ω to the SUBC OUT connector.
- Set synchronization to the INT mode.
- Adjust L2 for $2V_{PP} \pm 0.2V_{PP}$

2. Internal subcarrier amplitude.

- Connect an oscilloscope to $\textcircled{6}$.
- Set synchronization to the INT mode.
- Adjust L3 for maximum amplitude (approx. $2V_{PP}$).

3. Chroma amplitude.

- Connect an oscilloscope to $\textcircled{1}$.
- Connect a nominal video signal to the EXT SYNCHR connector.
- Set synchronization to the EXT mode.
- Adjust L1 for maximum amplitude (minimum $2V_{PP}$).

4. Subcarrier phase detector balance.

- Connect an oscilloscope to $\textcircled{4}$
- Connect a nominal video signal to the EXT SYNCHR connector.
- Set synchronization to EXT mode.
- Trigger the oscilloscope with a fv-pulse from the Test signal generator.
- Adjust R68 for minimum peak during the field pulse.

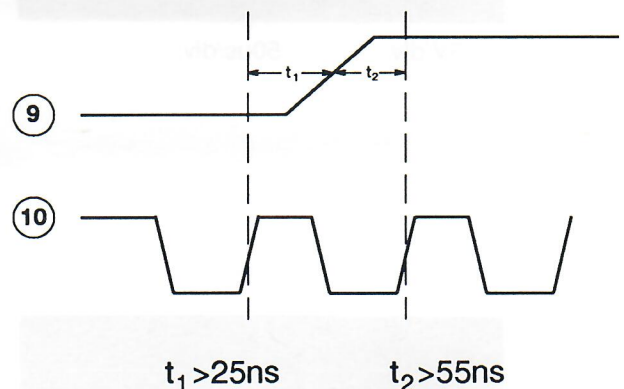
5. Line/Subc phase

- Connect a Sc-H meter terminated with 75Ω to either VIDEO OUT connector.
- Check that the Line/Subc phase is 0° .
- If not, adjust R140.

6. Clock timing

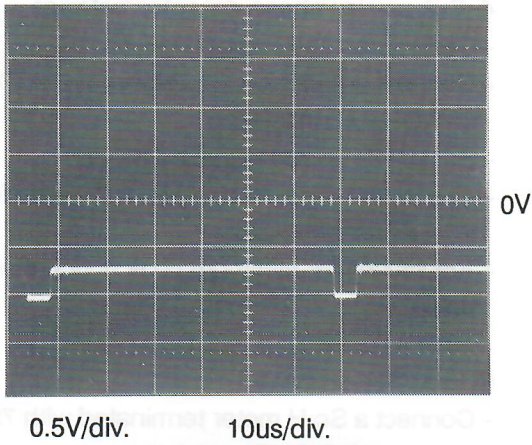
Only in case the SAA1043 has been replaced.

- Connect the oscilloscopes CH-A to $\textcircled{9}$ and CH-B to $\textcircled{10}$ (ground lead to $\textcircled{8}$).
- Check that the leading edge of signal $\textcircled{9}$ is located more than 25ns after and more than 55ns before the leading edge of $\textcircled{10}$ measured at the signals 2V crossing (see below).
- If not OK, move the jumper S13 to its opposite position and repeat the test.

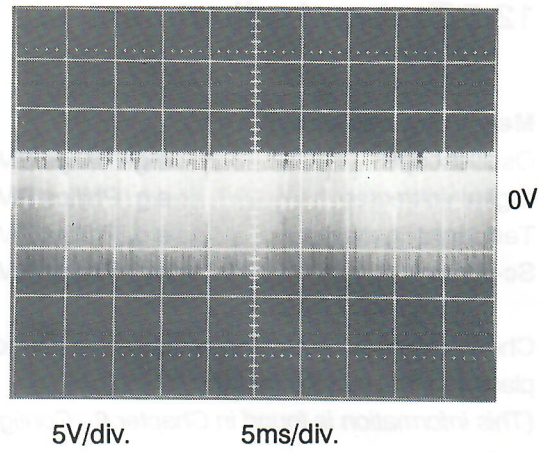


Clock timing

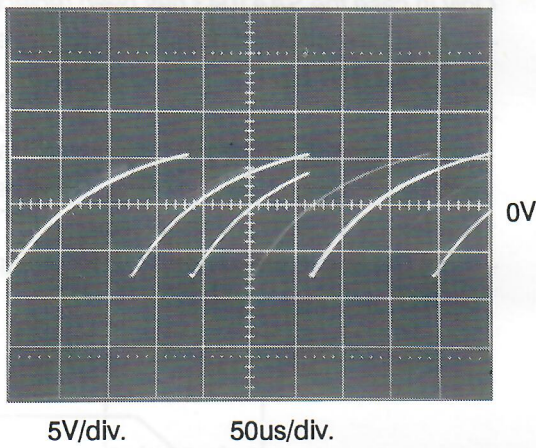
1



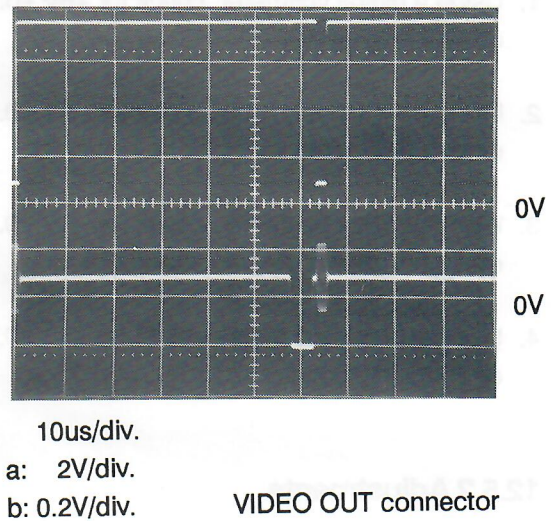
2



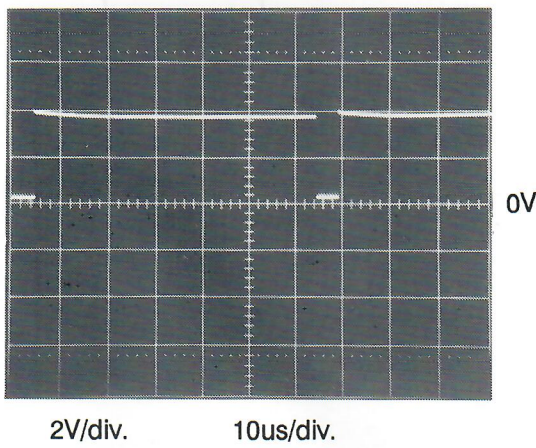
2



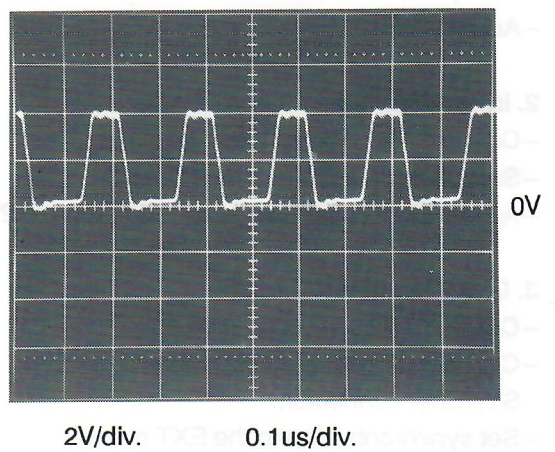
3

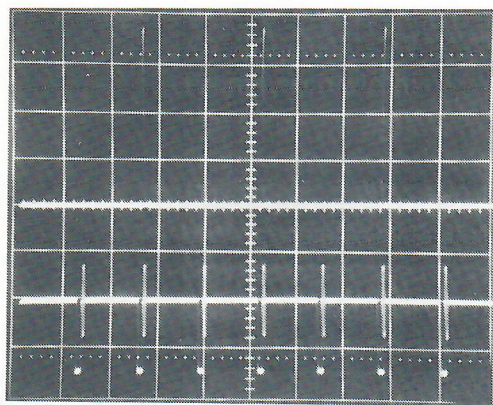


4



5





0V

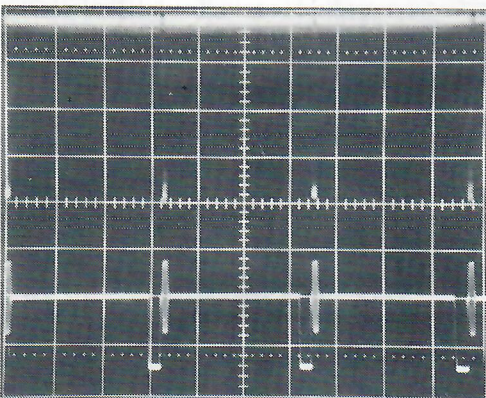
50us/div.

a: 2V/div.

b: 0.2V/div.

VIDEO OUT connector

EXT. SYNC provided



0V

0V

20us/div.

a: 100mV/div.

b: 0.2V/div.

VIDEO OUT connector

EXT. SYNC provided

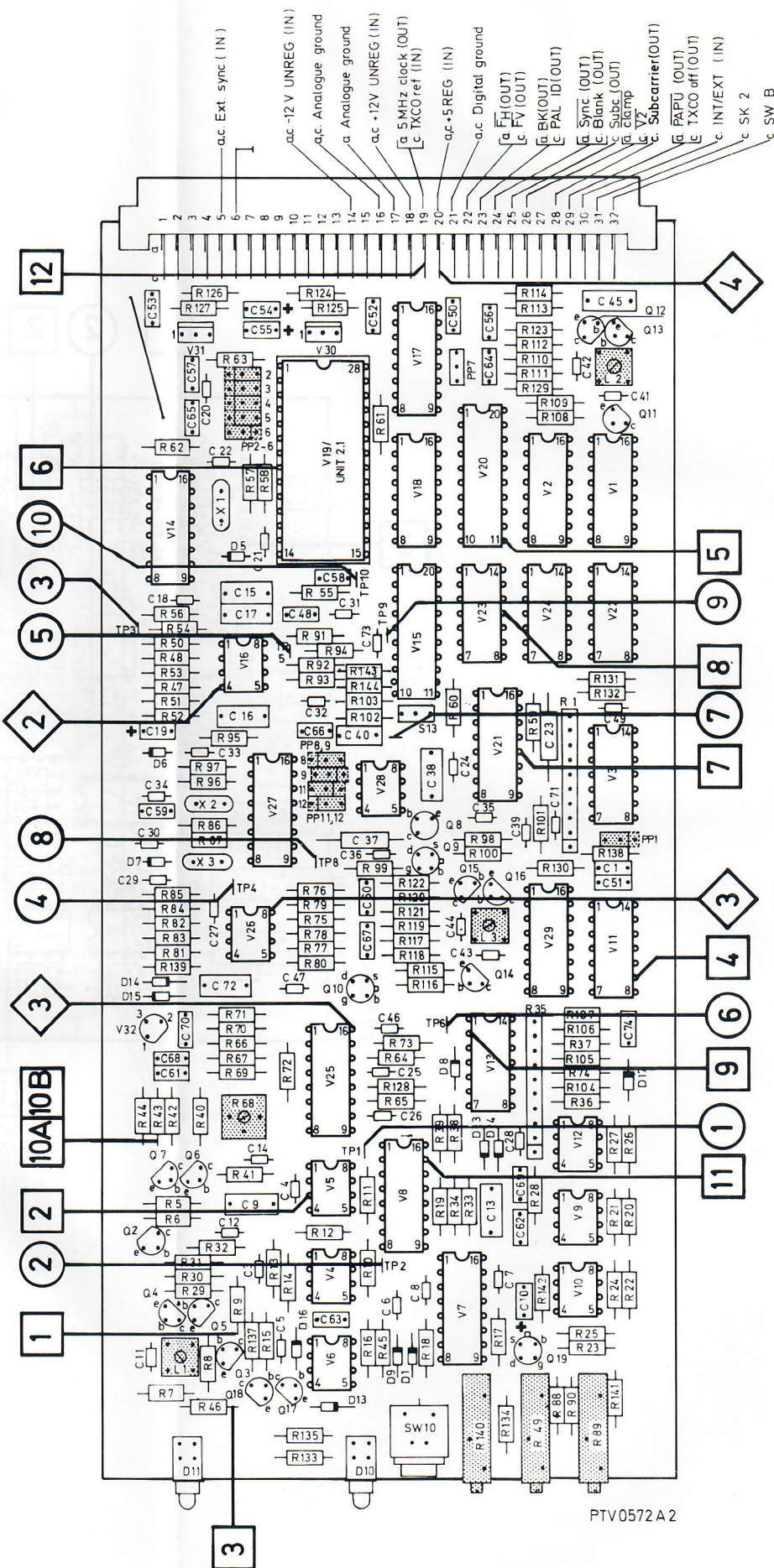
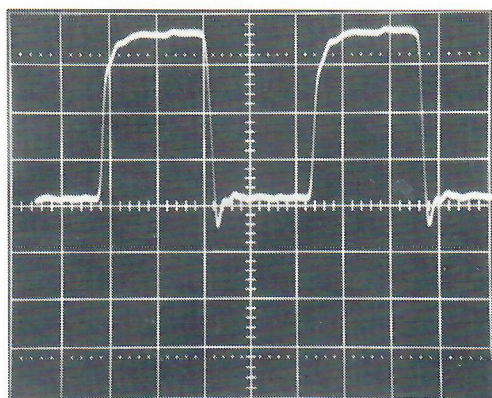


Fig. 12-5 Adj. elements, sync generator - unit 2

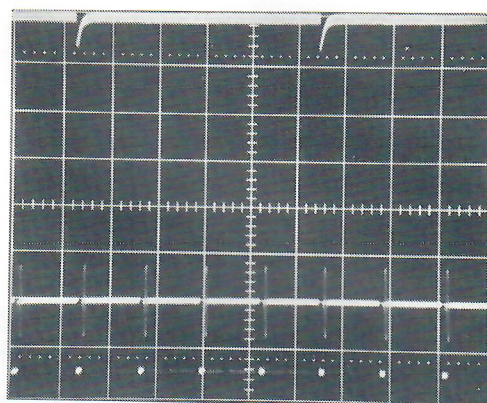
6



2V/div.

0.2 μ s/div.

7

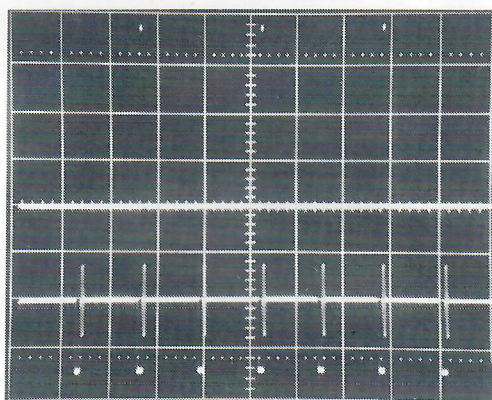
50 μ s/div.

a: 1V/div.

b: 0.2V/div.

VIDEO OUT connector

9

50 μ s/div.

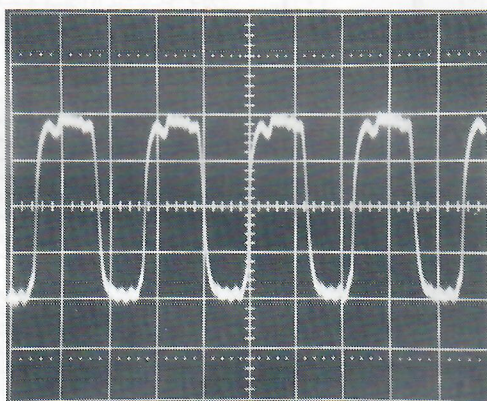
a: 2V/div.

b: 0.2V/div.

VIDEO OUT connector

EXT. SYNC provided

10A



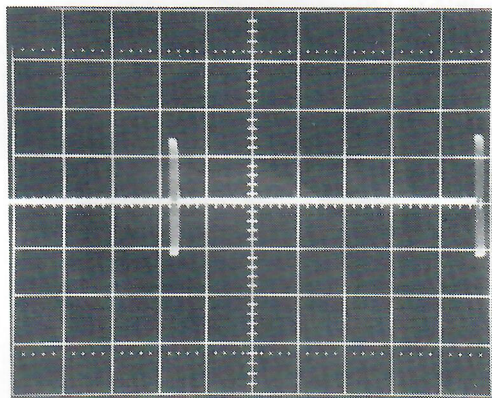
100mV/div.

0.1 μ s/div.

INT. SYNC

10B

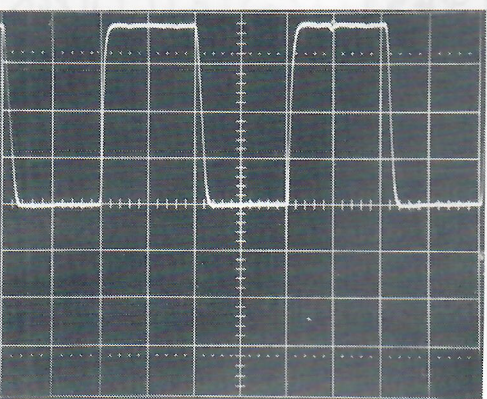
11



1V/div.

10 μ s/div.

12



1V/div.

0.5 μ s/div.

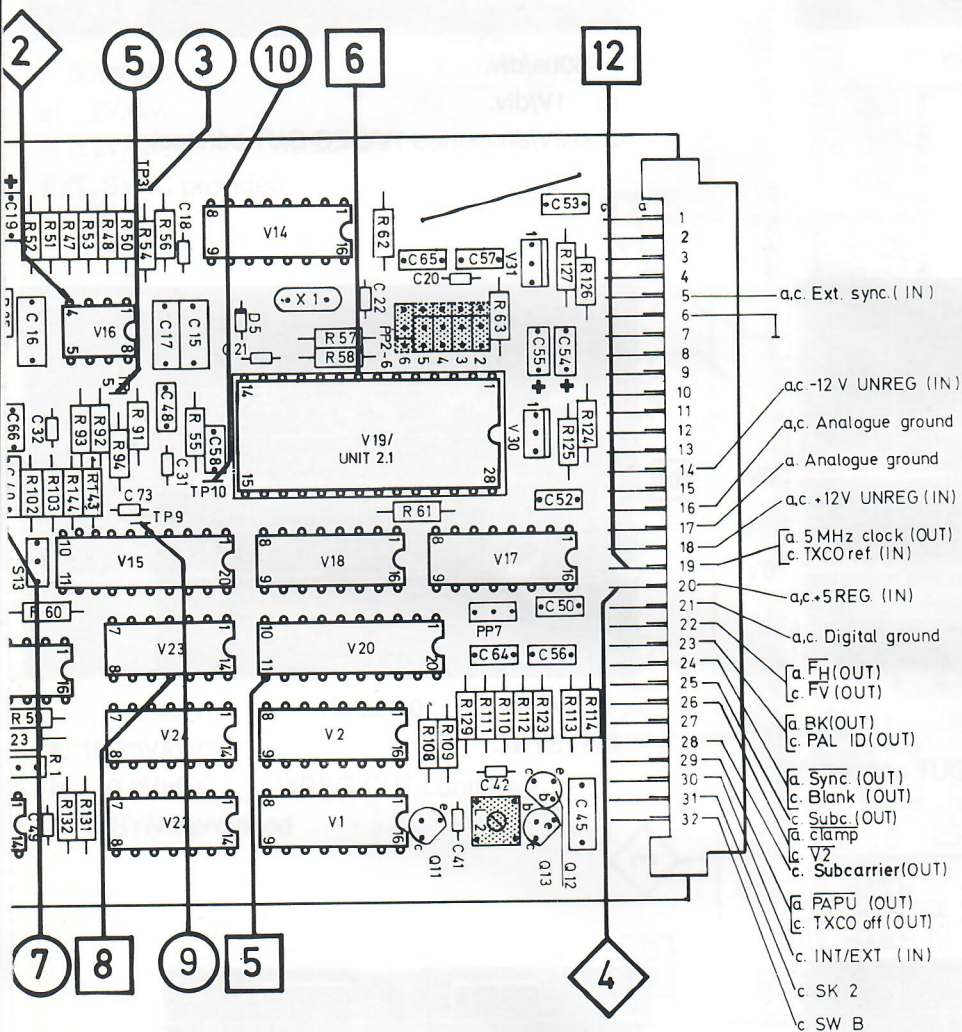


Fig. 12-6 Checkpoints, sync generator - unit 2

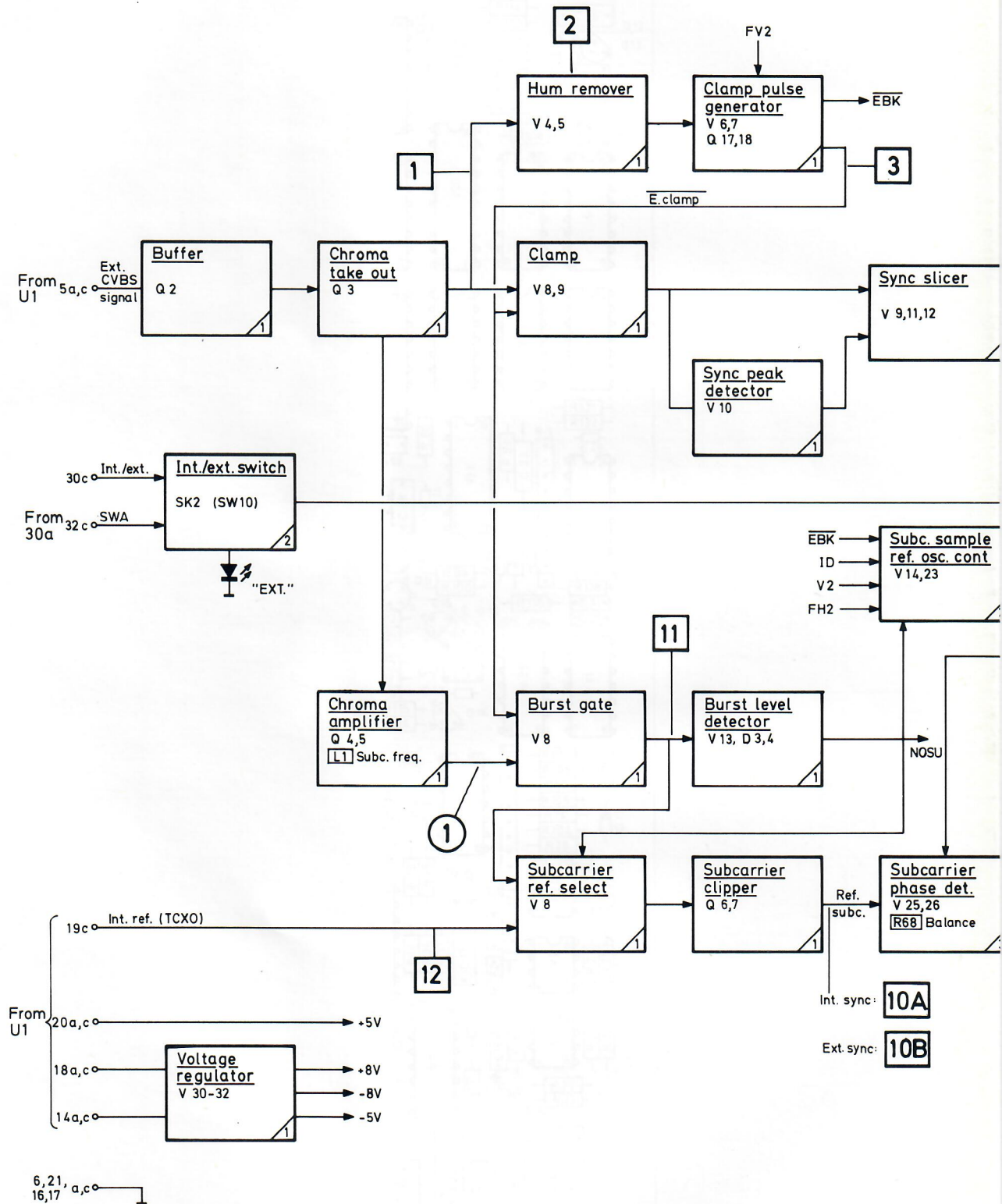
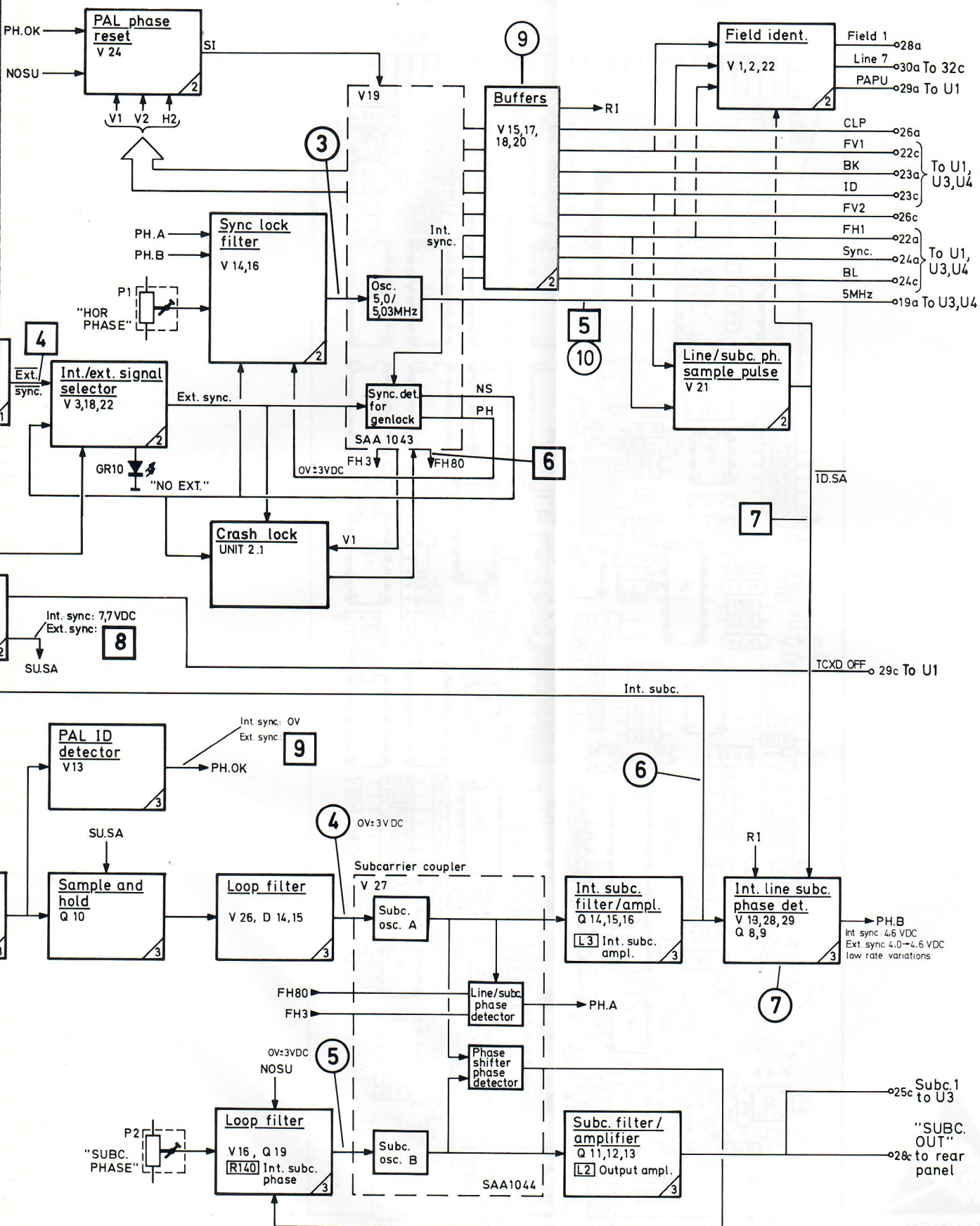


Fig. 12-7 Block diagram, sync generator - unit 2



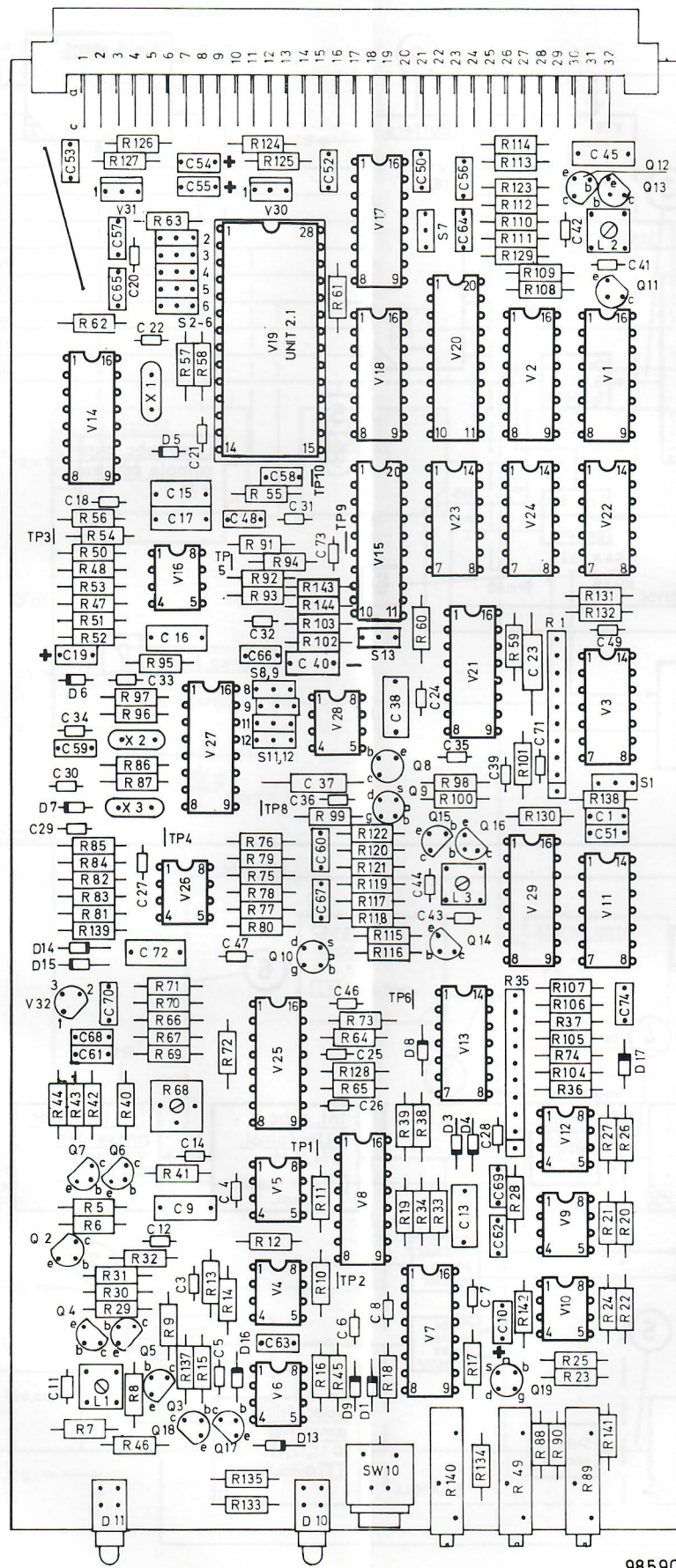


Fig. 12-9 Component location, sync generator - unit 2

BURST LEVEL DET.

[illegible]

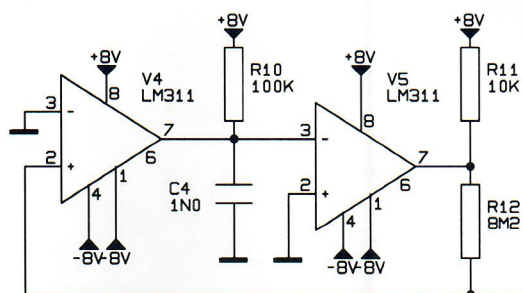
SUBC CLIPPER

The circuit diagram shows a signal path starting from an input, passing through resistors R38 (3K01) and R39 (10K). The signal then enters the Y1 pin of a 4053 CMOS switch (V8-A). The VDD pin (12) is connected to +8V, and the VSS pin (11) is connected to -5V. The Z pin (14) is connected to a 100K resistor (R40) to +8V and a 3K01 resistor (R41) to ground. The output of the switch is connected to a 4N7 diode (C14) in series with a 4K75 resistor (R44) to -8V. The signal then passes through a 267 resistor (R42) to ground and a 10K resistor (R43) to +8V. The final output is labeled REF SUBC.

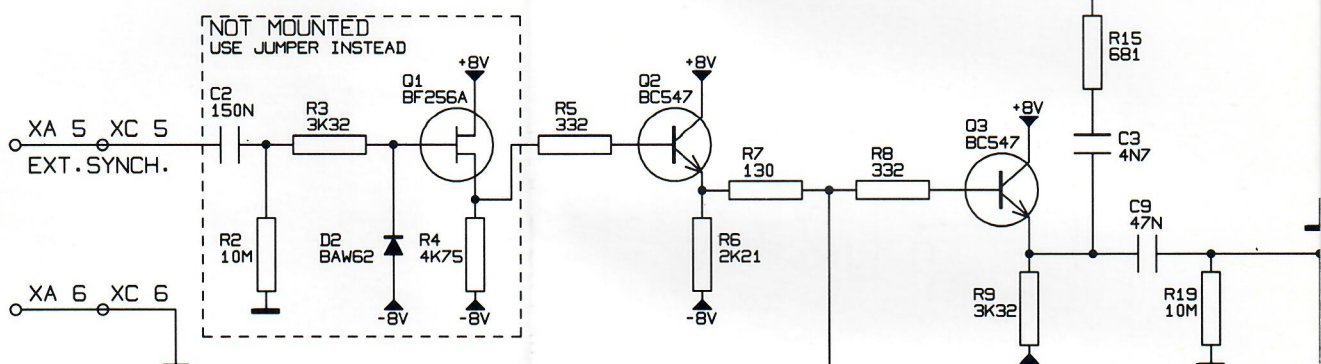
108 98590

Fig. 12-10 Circuit diagram, sync generator - unit 2, sh.1

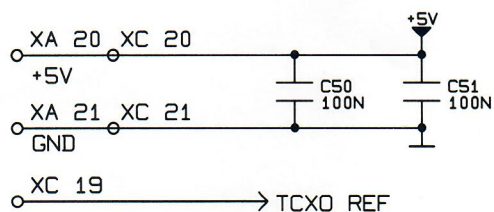
HUM REMOVER



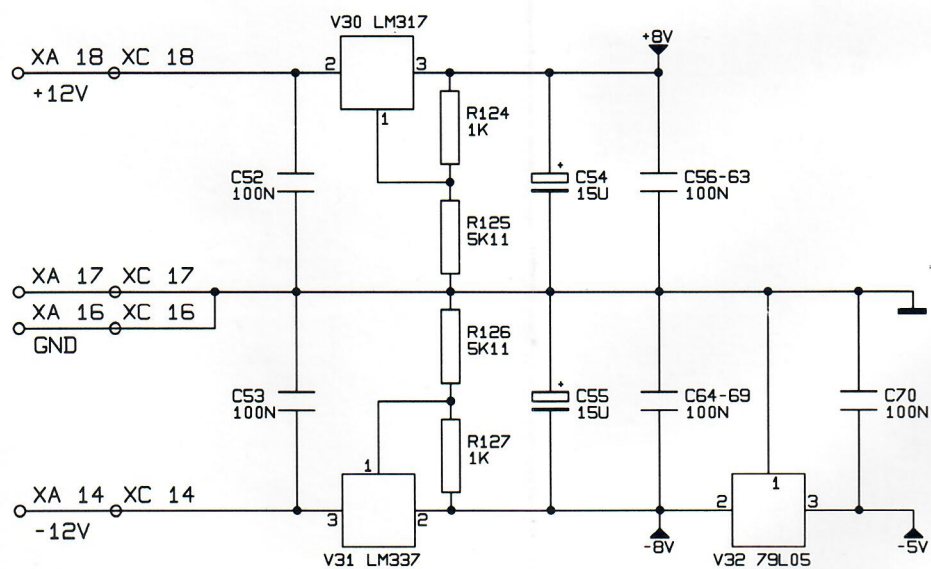
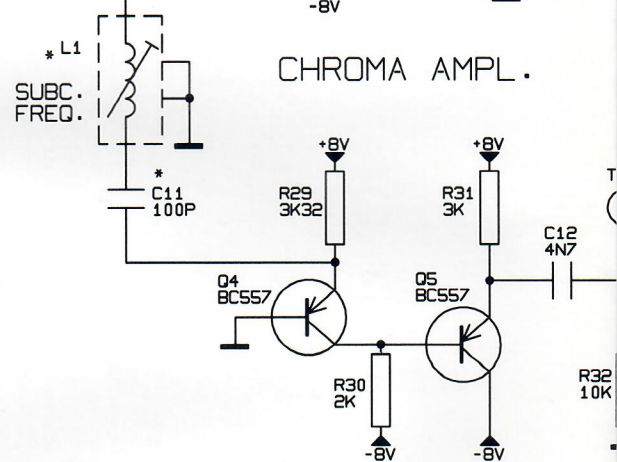
BUFFER



VOLTAGE REGULATORS

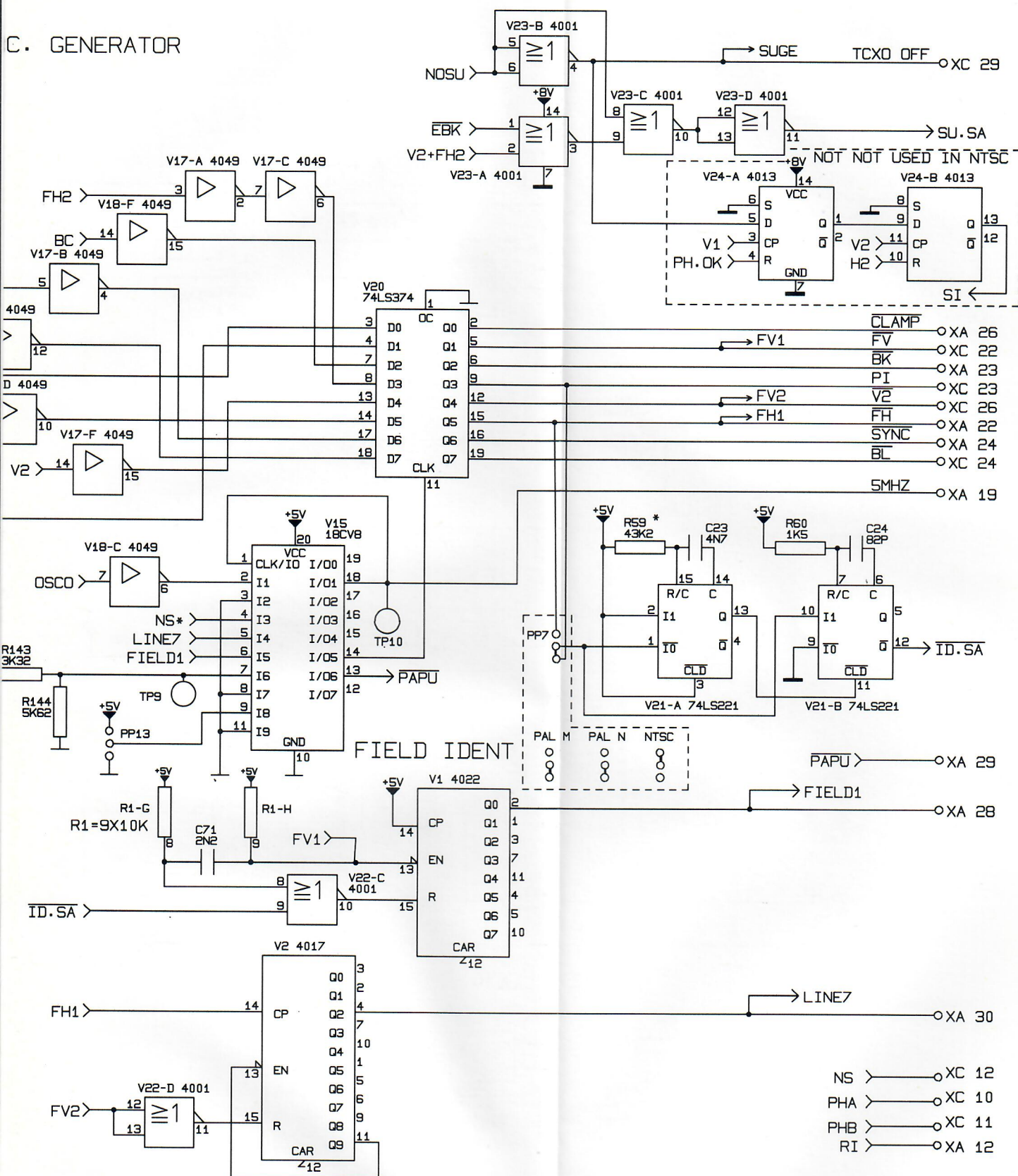


CHROMA AMPL.

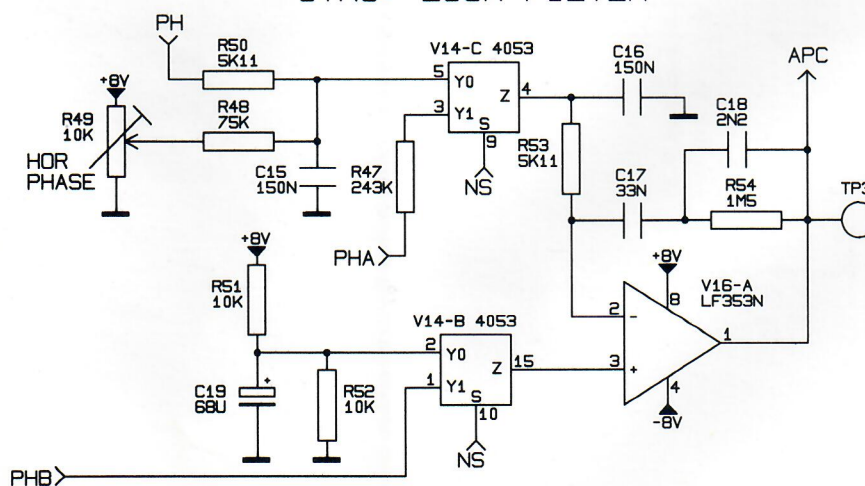


TCXO REF>

C. GENERATOR



* DEVIATING VALUES FOR OTHER VERSIONS
** NOT MOUNTED



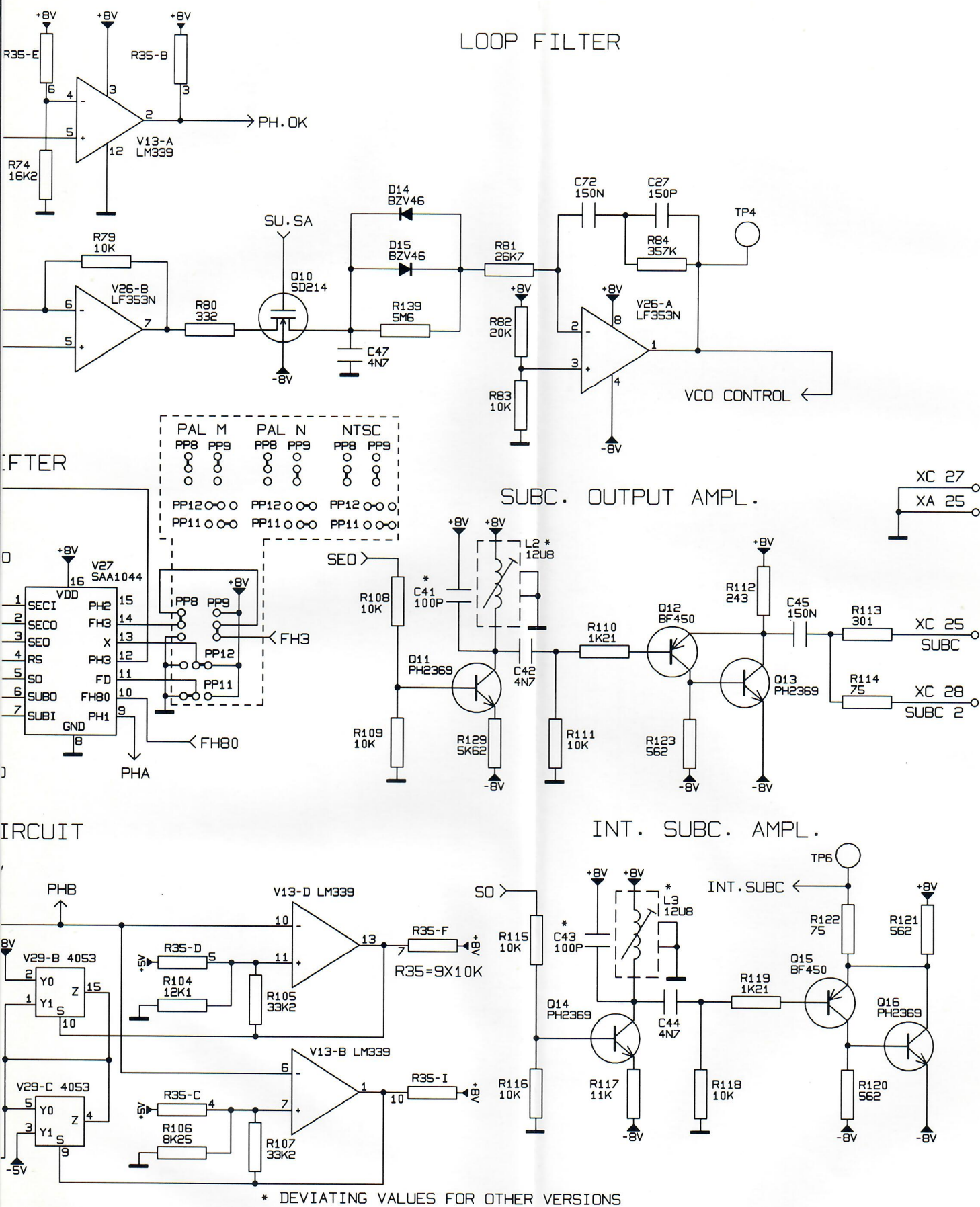
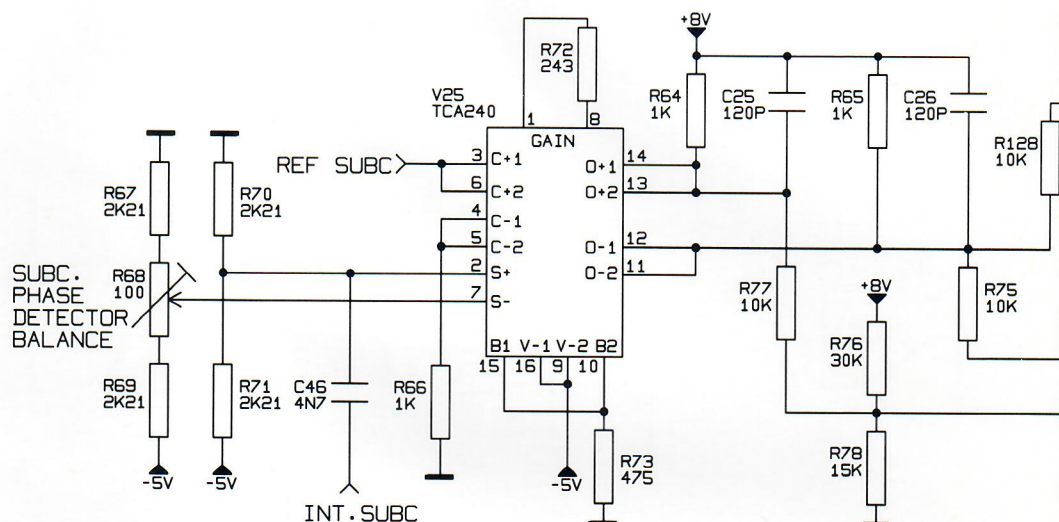
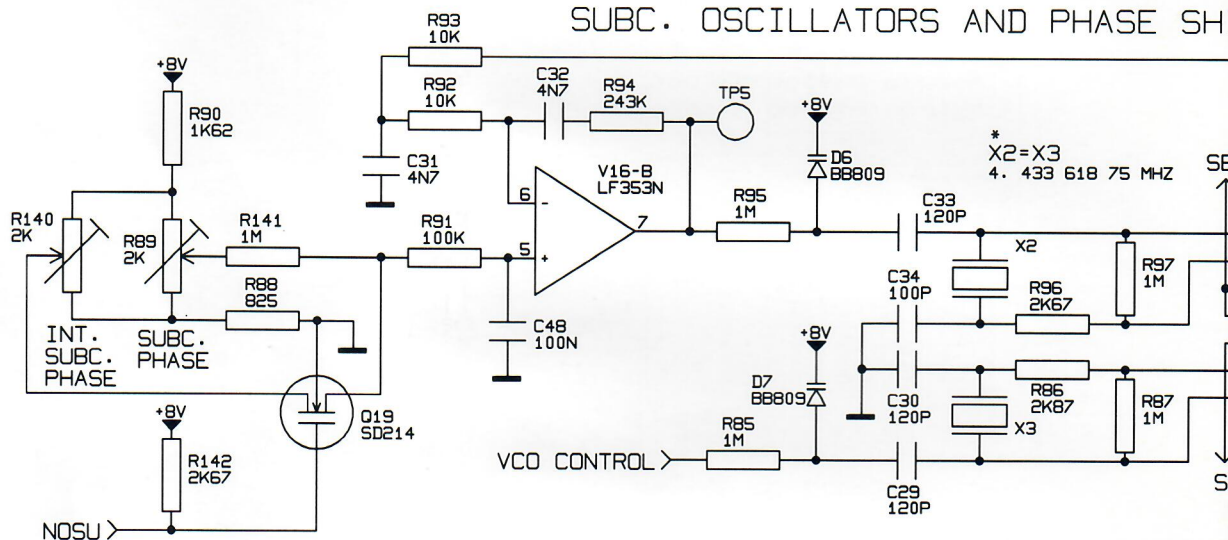


Fig. 12-12 Circuit diagram, sync generator - unit 2, sh.3

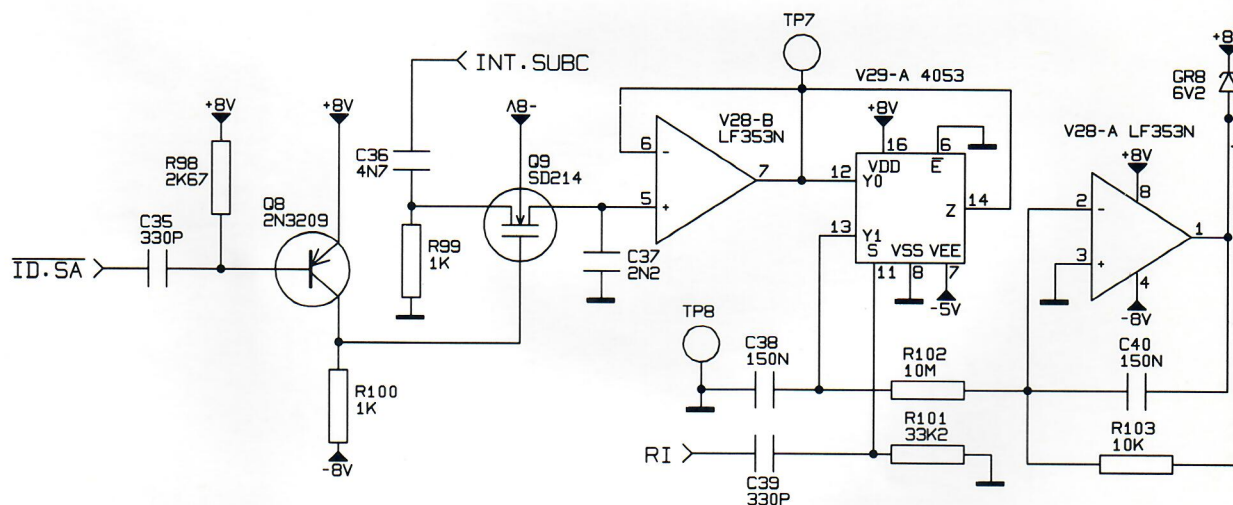
SUBC. PHASE DET.

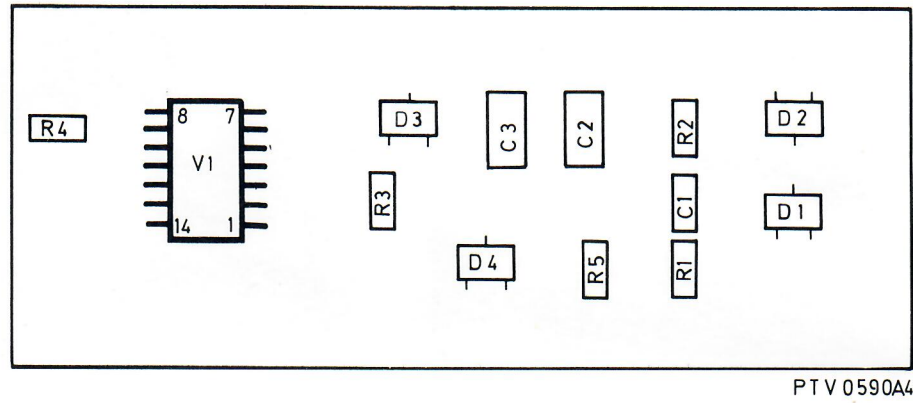


SUBC. OSCILLATORS AND PHASE SH



INT. LINE/SUBC.PHASE C





PTV 0590A4

Fig. 12-13 Component location, crash-lock unit - unit 2.1

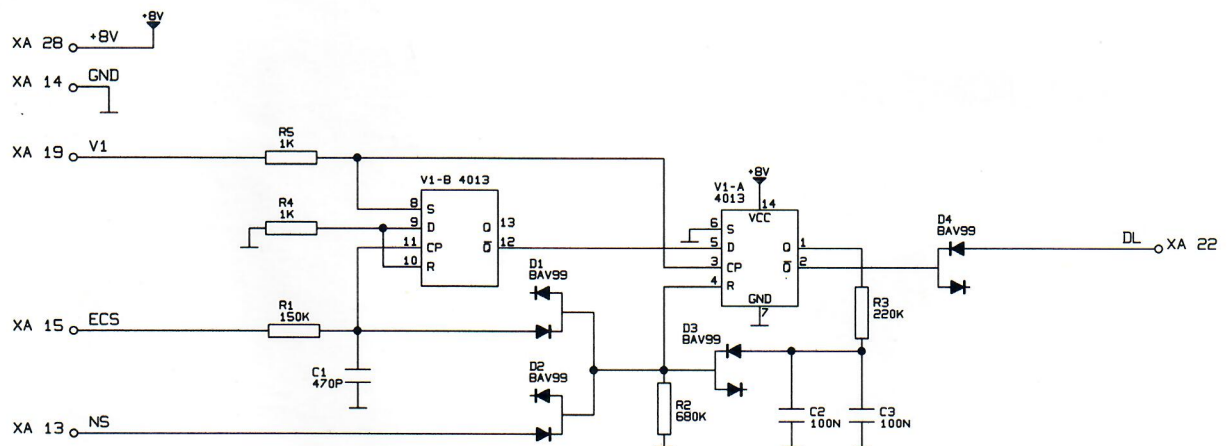


Fig. 12-14 Circuit diagram, crash-lock unit - unit 2.1